Bias and Frequency Dependence of FET Characteristics

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***Abstract*—A novel measurement of the dynamics of high electron-mobility transistor (HEMT) and MESFET behavior permits classification of rate-dependence mechanisms and identification of operating regions that they affect. This reveals a simple structure to the otherwise complicated behavior that has concerned circuit designers. Heating, impact ionization, and trapping contribute to transient behavior through rate-dependence mechanisms. These are illustrated by a simple description. Each has an effect on specific regions of bias and operating frequency. With this insight, it is possible to determine true isodyamic characteristics of HEMTs and MESFETs and to predict operating conditions that will or will not be affected by rate dependence. It is interesting to note that, for some devices, rate dependence can be seen to exist at microwave frequencies and may, therefore, contribute to intermodulation distortion.**

***Index Terms*—Charge carrier processes, impact ionization, MESFETs, microwave devices, MODFETs, pulse measurements, semiconductor device modeling.**

I. Introduction

The variation of high electron-mobility transistor (HEMT) and MESFET characteristics with operating condition (bias, temperature, and frequency) is significant for many applications. This is because the variations, invoked by the complex signals used in communication systems, result in undesired transient effects. With an improved understanding of the mechanisms involved, it should be possible to measure, quantify, and incorporate operating-condition dependency of FETs in the models used to simulate circuits. Better circuit designs will be possible because the extent of device variations and the conditions where they occur can be predicted.

Narrow pulses have been used to investigate the operating-condition dependency of FET characteristics [1]. The pulse measurements are applied to the normal operating regions of the device rather than outside the safe-operating area of breakdown regions, which is the traditional domain of previous pulse investigations. Provided the pulses are short enough, the data agree with small-signal RF measurements [2], though some devices have dependencies that require nanosecond resolution [3], [4]. A full characterization of operating-condition dependency over all bias points is inevitably limited by the shortest available pulse. Moreover, narrow pulses alone do not show the dynamics of the FET dependencies.

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It is necessary to use a technique involving dc, large-signal pulse, and small-signal RF measurements to fully identify the operating-condition dependency of FETs [5], [6]. This is described in Section II. This technique was used to study MESFET and HEMT characteristics over an extremely wide range of frequencies from dc to microwave and a wide range of bias and temperature. Measurements were made at temperatures ranging from 10 °C to 70 °C. The study used standard geometry devices at process control sites on wafers recently manufactured in commercial processes. The results are summarized in Section III and the implications are discussed in Section IV.

Self-heating [4] and charge trapping related to impact ionization [7], [8] and leakage currents [9] are known to contribute to the variation of FET characteristics. Each contribution is thought to have an effect at a specific range of operating conditions. Although a physical study of these mechanisms is not the subject of this paper, a simple descriptive model is proposed in Section V. This illustrates the mechanisms involved in the observed operating-condition dependency and provides the insight required to determine the true isodynamic characteristics of an FET.

II. Measurement of FET Dynamics

Steady-state characteristics, such as those of the HEMT shown in Fig. 1, have traditionally been used to describe transistor behavior. The measurements provide detailed characterization of bias conditions including gate current.

Pulse measurements, such as those shown in Fig. 2 for the same HEMT, show significant transient behavior that is better visualized as a time-evolution plot, such as shown in Fig. 3 [9]. These are the same characteristics shown in Fig. 2 over a continuum of time. Analysis of a comprehensive set of these measurements provides an understanding of the bias and time dependence of the FET characteristics. In particular, the journey from a starting bias point to any new bias point is observable.

The measured time-evolution characteristics in Fig. 3 are dominated by the *kink effect* that is coincident with the significant rise in gate current, shown in Fig. 1, caused by impact ionization. For a MESFET with little or no impact ionization, as indicated by a simple gate current characteristic, the time-evolution characteristics do not exhibit such a kink [5].

The large-signal time-evolution data are easily measured with pulse techniques for time periods greater than the fastest pulse measurement. Large-signal characteristics over shorter time periods are not resolvable. However, small-signal parameters can be measured with RF techniques. Transconductance and drain conductance determined numerically from pulse data

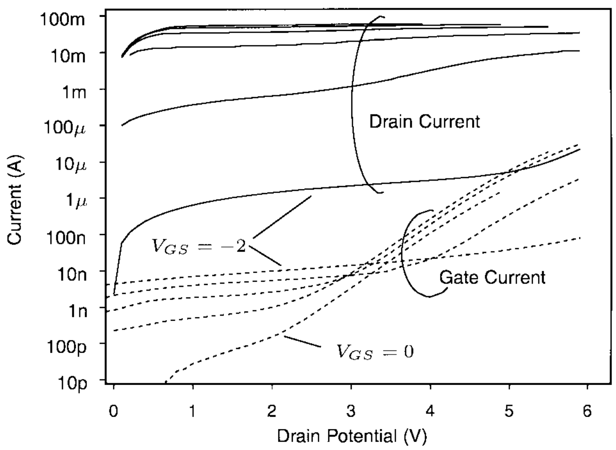

Fig. 1. Steady-state drain (—) and gate (- - -) current of an HEMT with V_{GS} from -2.0 to 0.0 V in 0.5-V steps as the parameter.

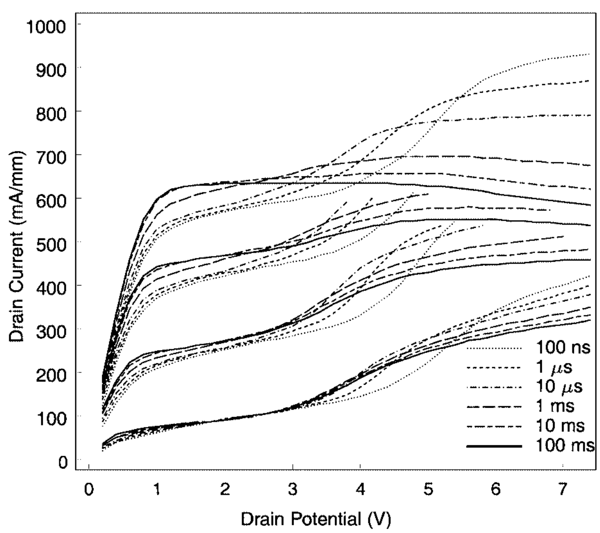

Fig. 2. Measured pulsed characteristics of the HEMT in Fig. 1 from the initial condition $V_{\mathrm{GS}} = -2.0$ V, $V_{\mathrm{DS}} = 1.2$ V with v_{GS} at -1.2, -0.8, -0.4, and 0.0 V as the parameter.

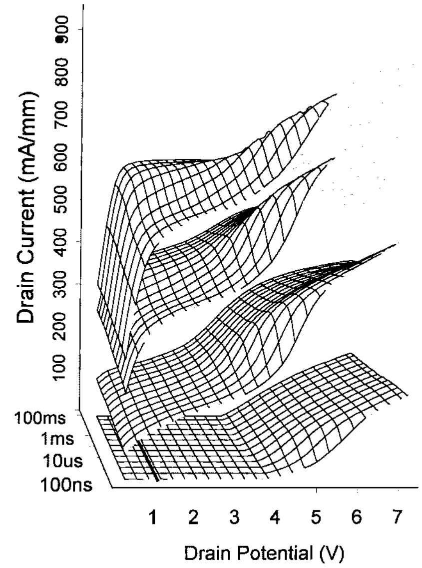

Fig. 3. Time-evolution view of the characteristics shown in Fig. 2.

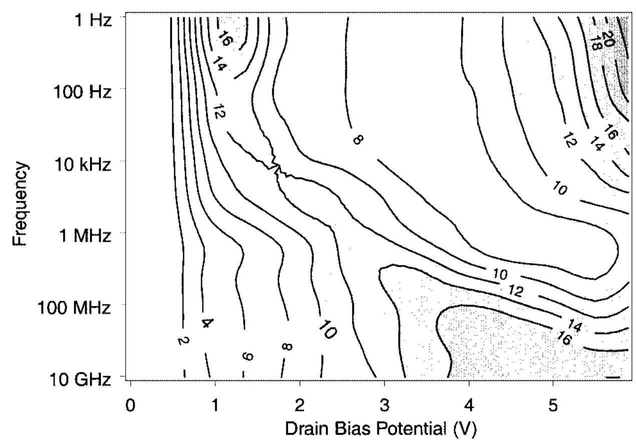

Fig. 4. Intrinsic gain versus drain bias for the HEMT in Fig. 1 operating at 25 °C with $V_{\mathrm{GS}} = -0.4$ V. Darker areas correspond to regions of higher gain.

can be combined with data from RF measurements to obtain small-signal parameters from dc to microwave frequencies. The results can be usefully presented in terms of intrinsic gain (transconductance divided by drain conductance) as a function of operating condition. Although this measurement is limited to small-signal parameters and necessarily considers many biases rather than a single bias, it provides a comprehensive measurement of the rate-dependence mechanisms of FETs.

III. Intrinsic Gain

The intrinsic gain over ten decades of frequency from 1 Hz to 10 GHz, or in time from 160 ms down to 16 ps, is shown in the contour map of Fig. 4. For each bias point, the small-signal parameters were derived from pulse data measured with an enhanced arbitrary pulsed semiconductor parameter analyzer (APSPA) [4] for frequencies below 1 MHz, and from Y-parameters measured with a network analyzer for frequencies above 1 MHz [5].

There is a significant variation in gain over frequency and drain bias potential. The gain peaks in the knee region at very low frequencies and at higher drain potentials. The gain would normally be just as high at intermediate drain bias potentials if it were not for a significant rate dependency. This rate dependency reduces gain at low frequencies near a bias of 3.5 V and at higher frequencies for higher bias potentials. This reduction in gain can be directly related to the kink in the pulsed-*I/V* characteristics of Figs. 2 and 3, which occurs at slower times near the 3.5-V drain potential, and faster times at higher potentials.

Measurements over various gate biases and temperatures give similar intrinsic gain contour maps with changes in the position and size of the peaks and troughs. There is no remarkable change in the general shape of the contours with change in temperature. Low-frequency gain decreases with gate bias, while the high-frequency gain is largely unaffected. Low-frequency gain increases with temperature, while high-frequency gain decreases. Changes in temperature and gate bias always affect the knee region, especially at low frequencies. There is little change at high drain bias.

The intrinsic gain for the MESFET, which does not exhibit impact ionization, has a simpler structure dominated by thermal and electron trapping effects. The intrinsic gain at high power dissipation can be very large at extremely low frequencies ($<$100 Hz) because the drain conductance is near or less than zero. Variation with gate bias and temperature is not dramatic.

Of note is that, for both the MESFETs and HEMTs, there exists a region of isodynamic characteristics above 1 MHz for low drain potentials. That is, in this region, the gain remains essentially independent of frequency. Also of note is that, at high drain potentials, the rate dependency affects the gain at microwave frequencies.

IV. Rate-Dependence Mechanisms

The rate dependencies shown in Fig. 4 can be explained by many mechanisms. The three dominant mechanisms considered here are: 1) a change in drain current due to a self-heating effect; 2) a change in effective gate potential due to a potential of electron traps; and 3) a change in effective gate potential due to a potential of hole traps [5]. The currents that supply charge to the traps are, in themselves, an insignificant contribution to the drain current. However, the potential of the traps has a significant influence on the drain current through the transconductance of the device. The nature and location of these traps within the device is not considered here.

Consider the self-heating effect alone. The thermal effect, evident in both the MESFET and HEMT at high power levels, stems from heating due to power dissipation. At very high frequencies, the temperature of the device is set by the bias and the gain is that of the FET for the corresponding temperature. At audio frequencies ($<$ 10 kHz), the average power dissipation and, hence, temperature, varies with the signal. The variation of temperature over the course of a signal swing reduces the output conductance, which increases the gain. For sufficiently high levels of power dissipation, the output conductance and, hence, gain, becomes negative at extremely low frequencies.

Consider the effect on the intrinsic gain of electron traps alone. At very high frequencies, the gain is not significantly affected because the trap potential remains constant relative to the signal. At low frequencies, the trap potentials change with the signal. There is usually a significant trap potential that can be linked to gate–drain potential. As the gate–drain potential $V_{\rm GD}$ becomes more negative, so does the trap potential. An increase in drain potential gives a more negative trap potential that reduces the drain current. Thus, the drain conductance is reduced, which increases gain. This effect is the principal cause of *drain overshoot* and the converse is the cause of *gate lag*. The frequency at which gain increases varies with drain bias. This suggests that the trap occupancy rate increases with bias.

Consider the effect on the intrinsic gain of hole traps alone. It is assumed that the trapped holes stem from impact ionization, evident in the HEMT. As is the case with the other rate-dependence mechanisms, the gain is not significantly affected at very high frequencies because the trap potential remains constant. At low frequencies, the trap potential does change with the signal and there is a significant reduction in intrinsic gain. The reduction is most pronounced in the region of the kink in the drain characteristic, which is exactly what would be expected from the corresponding large increase in drain conductance. The frequency at which this occurs is linked to the magnitude of the impact ionization current and, hence, to the drain bias. The many orders of magnitude increase in gate current indicates significant impact ionization at high drain bias. This is accompanied by rate dependency at microwave frequencies.

An understanding of the rate-dependence mechanisms can give an insight into the effects of bias, temperature, and frequency on the characteristics of an FET. For example, the shift in gain of an FET with temperature can be determined from appropriate intrinsic gain contour maps. Increasing temperature shifts the intrinsic gain contour map in a similar way as lowering the gate bias. This is to be expected because either change will increase the occupancy rate of traps, which has the effect of simply shifting the trap-related rate dependency of FET characteristics to higher frequencies. With this understanding, the bias and temperature variation can be inferred from a single intrinsic gain contour map. If the operating bias and frequency were in a relatively flat region of the contour map, then little variation with temperature or bias would be expected, whereas an operating point in a sloping region will be sensitive to temperature or bias changes.

V. Illustrative Model

The following is a simplified presentation of a description of thermal and trapping mechanisms [5]. It is simply for illustration and not an FET circuit model. It does, however, explain the dynamics involved and their influence on the characteristics.

The following simple drain current model serves as an adequate basis for the description:

$$i_{\rm DS} = \beta {v_C}^2 (1 - \delta \overline{p}) \tanh(\alpha v_{\rm DS}) \tag{1}$$

$$v_C = v_{\rm GS} + \gamma v_{\rm DS} - \overline{v_E} + \overline{v_H} - V_T \tag{2}$$

where the fitting constants are the transconductance parameter β A $\cdot$ V^{-2}, saturation potential α V^{-1}, pinchoff potential V_T V, and gain parameter γ. The remaining parameters control the influence of power dissipation and additional controlling potentials from traps. The *thermal resistance-temperature coefficient* δ K/W$\cdot$K sets the reduction in drain current with average power dissipation $\overline{p}$. The terms $\overline{v_E}$ and $\overline{v_H}$ are the effective electron trap and hole trap potentials, respectively.

Average power dissipation and effective trap potentials are dynamically determined by first-order differential equations

$$i_{\rm DS} v_{\rm DS} = \overline{p} + \tau_\delta \frac{d}{dt} \overline{p} \tag{3}$$

$$V_H \ln(f_{II} + 1) = \overline{v_H} + \tau_H \frac{1}{f_{II}} \frac{d}{dt} \overline{v_H} \tag{4}$$

$$\gamma_E v_{DG} = \overline{v_E} + \tau_E e^{-v_{DG}/V_B} \frac{d}{dt} \overline{v_E} \tag{5}$$

where

$$f_{II} = \exp\left(\frac{-B}{v_{\rm DS} - V_S + \sqrt{(v_{\rm DS} - V_S)^2 + 2}} \right) \tag{6}$$

is a factor related to impact ionization rate. The constant V_S V is the critical drain potential for onset of impact ionization, γ_E, V_H V, B V and V_B V are fitting constants.

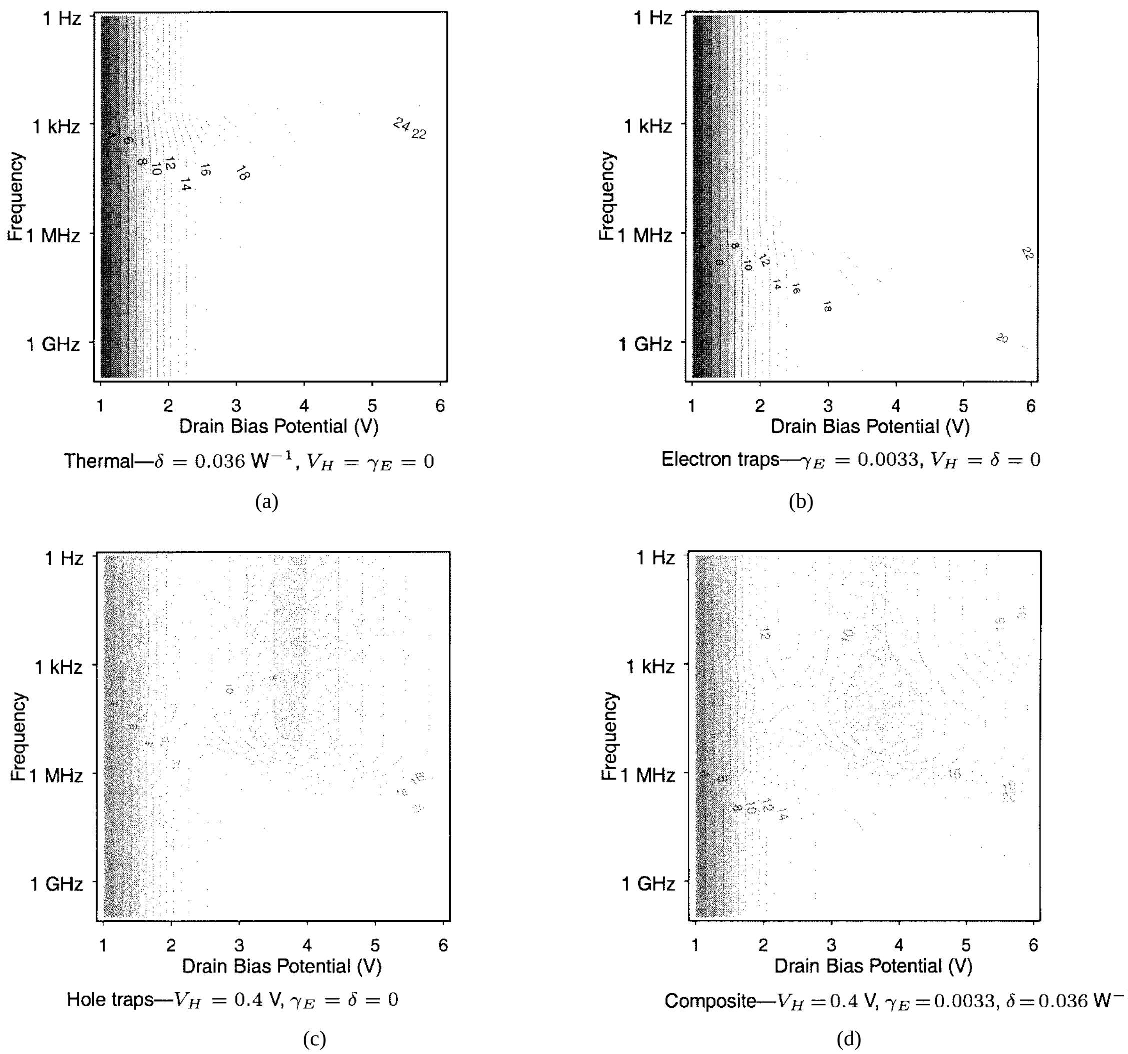

Fig. 5. Illustration of the influence of thermal and trapping effects on the intrinsic gain of an FET as a function of drain bias and frequency at $V_{\mathrm{GS}} = -0.5$ V. Equations (1)–(6) were used with parameters $\alpha = 1.05$ V^{-1}, $B = 1.25$ V, $\beta = 0.4$ A $\cdot$ V^{-2}, $\gamma = 0.04$, $V_B = 0.7$ V, $V_S = 3.5$ V, $V_T = -1.5$ V, and time constants $\tau_\delta = 100$ μs, $\tau_E = 2$ μs, and $\tau_H = 50$ ns.

The average power is determined from instantaneous power over a time-constant τ_δ s, which is determined by the physical structure of the thermal path from the device. It is, therefore, assumed constant with respect to electrical conditions.

The rate of trap potential change is a function of bias. Thus, the time constant for the effective electron trap potential τ_E s, is multiplied by an exponential function of gate–drain bias, and the time constant for the effective hole trap potential τ_H s, is multiplied by the impact ionization factor. The generation and recombination rates are simply assumed to be equal in this description.

The illustrative description was used to simulate the intrinsic gain of a representative device over a plane of drain potential and frequency. The results of this are shown in Fig. 5, which depicts the effect of thermal and trapping effects individually and together.

Despite the simplicity of this description, the simulation of intrinsic gain affected by these three rate-dependence mechanisms, shown in Figs. 5(d) and 6, has the characteristics of the real device shown in Figs. 4 and 7. A better description would require consideration of heating through a distributed conduc-

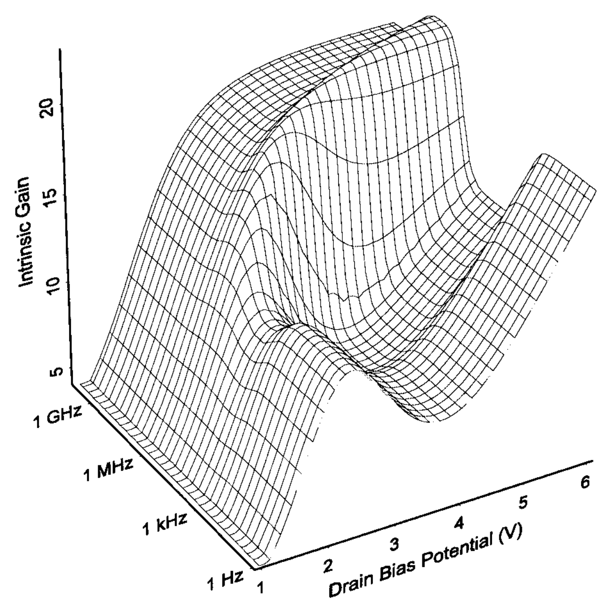

Fig. 6. Three-dimensional view of the calculated gain in Fig. 5(d).

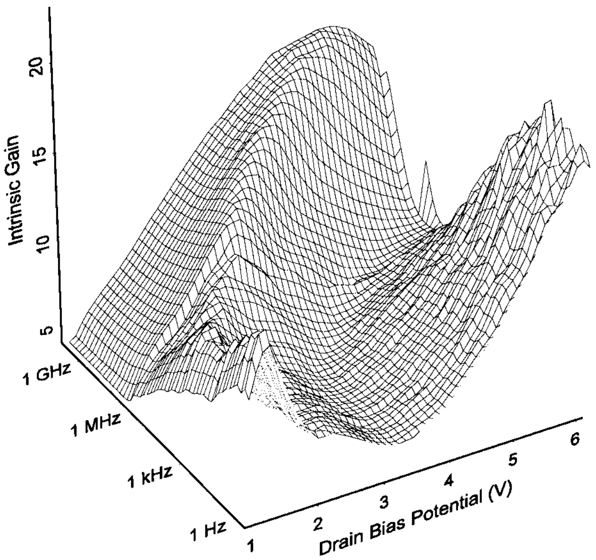

Fig. 7. Measured intrinsic gain of the HEMT in Fig. 1 at $V_{\rm GS} = -0.5$ V.

tion path to ambient, a more accurate description of trapping at low drain potentials, and a more detailed description of impact ionization. It is also likely that there are other traps and mechanisms that may need to be considered.

However, this description explains the structure of a measured intrinsic gain contour map. It predicts that the trapping effects are significant at microwave frequencies when operating at higher drain potentials. It also predicts an isodynamic region of operation at low drain potentials and sufficiently high frequency. In this region, the gain is independent of frequency and is not sensitive to moderate changes in temperature and gate bias.

VI. Conclusion

A technique for measuring intrinsic gain over a wide range of bias, temperature, and frequencies has given a comprehensive view of the effect of rate-dependence mechanisms on FET characteristics. These effects are adequately explained in terms of heating that reduces current, impact ionization that produces a kink in the characteristics, and electron trapping. A simple description of an FET that incorporates these mechanisms can replicate the structure of a contour map of measured intrinsic gain versus frequency and bias.

Intrinsic gain is proposed as a figure-of-merit that is invaluable for assessing the impact of the rate dependence on circuit performance. It is indicative of the bias, temperature, and frequency dependence of the device. Flat regions of a gain contour map will be less sensitive to these effects. For certain bias points, however, the gain varies significantly as a function of frequency up to microwave rates. This will be sensitive to temperature and bias variations. These regions can also have a variation in gain at the various frequencies of a multitone signal that may affect the level of intermodulation. This effect on distortion and intermodulation should be investigated.

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